



EL169860305

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Flash Memory And Method Of Forming Flash Memory

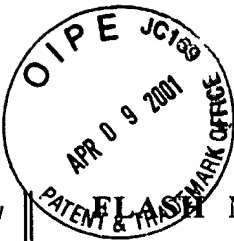
* * * * *

INVENTOR

Graham Wolstenholme

ATTORNEY'S DOCKET NO. MI55-001

09768878-040901



FLASH MEMORY AND METHOD OF FORMING FLASH MEMORY

TECHNICAL FIELD

This invention relates generally to FLASH memory and methods of forming FLASH memory.

BACKGROUND OF THE INVENTION

Memory is but one type of integrated circuitry. Some memory circuitry allows for both on-demand data storage and data retrieval. For example, memories which allow both writing and reading, and whose memory cells can be accessed in a random order independent of physical location, are referred to as random-access memories (RAM). Read-only memories (ROMs) are those in which only the read operation can be performed rapidly. Entering data into a read-only memory is typically referred to as programming, and the operation is considerably slower than the writing operation utilized in random-access memory. With random-access memory, information is typically stored with respect to each memory cell either through charging of a capacitor or the setting of a state of a bi-stable flip-flop circuit. With either, the stored information is destroyed when power is interrupted. Read-only memories are typically non-volatile, with the data being entered during manufacturing or subsequently during programming.

1 Some read-only memory devices can be erased as well as written
2 to by a programmer. Erasable read-only memory typically depends on
3 the long-term retention of electronic charge as the information storage
4 mechanism. The charge is typically stored on a floating semiconductive
5 gate, such as polysilicon. One type of read-only memory comprises
6 FLASH memory. Such memory can be selectively erased rapidly
7 through the use of an electrical erase signal.

8 A FLASH memory cell typically comprises a single floating gate
9 transistor. For multiple storage cells, such as used in large
10 semiconductor memories, the storage cells of the memory are arranged
11 in an array consisting of rows and columns. The rows are typically
12 considered as comprising individual conductive gate lines formed as a
13 series of spaced floating gates received along a single conductive line.
14 Source and drain regions of the cells are formed relative to active area
15 of a semiconductor substrate, with the active areas being generally
16 formed in lines running substantially perpendicular to the lines of
17 floating gates. The sources and drains are formed on opposing sides
18 of the lines of floating gates within the active area with respect to
19 each floating gate of the array. Thus, lines (rows) of programmable
20 transistors are formed.

21 Electrical connections are made with respect to each drain to
22 enable separate accessing of each memory cell. Such interconnections
23 are arranged in lines comprising the columns of the array. The sources
24 in FLASH memory, however, are typically all interconnected and

09758878-040901

provided at one potential, for example ground, throughout the array. Accordingly, the source regions along a given line of floating gates are typically all provided to interconnect within the substrate in a line running parallel and immediately adjacent the line of floating gates. These regions of continuously running source area are interconnected outside of the array, and strapped to a suitable connection for providing the desired potential relative to all the sources within the array. Accordingly, prior art techniques have been utilized to form a line of continuously running implanted source material within the semiconductor substrate and running parallel with the floating gate word lines.

In a principal technique of achieving the same, the substrate has first been fabricated to form field oxide regions by LOCOS. The fabrication forms alternating strips of active area and LOCOS field oxide running substantially perpendicular to the floating gate word lines which will be subsequently formed. Thus running immediately adjacent and parallel with the respective word lines will be an alternating series of LOCOS isolation regions and active area regions on both the source and drain sides of a respective line of floating gates. After forming the lines of floating gates and to provide a continuous line of essentially interconnected source regions, the substrate is masked to form an exposed area on the source side of the respective lines of floating gates. The LOCOS oxide is then selectively etched relative to the underlying substrate. This leaves a series of spaced trenches along the

0976878 2489760

1 lines of floating gates the result of removal of oxide from the
2 previously oxidized substrate which formed the LOCOS regions.

3 Non-recessed LOCOS in fabrication of FLASH memory in this
4 manner is typically very shallow relative to the semiconductor substrate
5 (i.e., less than 1500 Angstroms deep). This leaves a gradual, almost
6 sinusoidal, undulating surface of exposed semiconductor substrate running
7 in lines substantially parallel and immediately adjacent the lines of
8 floating gates on the desired source side. With the gently sloping
9 sidewalls of the trenches or recesses left by the LOCOS oxide removal,
10 one or more source ion implant steps are conducted through the mask
11 openings of the remaining photoresist layer. The result is formation of
12 a continuously and conductively doped source line within the
13 semiconductor substrate immediately adjacent the line of floating gates.

14 Circuitry fabrication and isolation of adjacent circuitry within a
15 semiconductor substrate can also be achieved with a trench isolation
16 that is different from LOCOS. For example, trenches can initially be
17 etched within a semiconductor substrate and subsequently filled with an
18 insulating material, such as high density plasma deposited oxide. Such
19 trenches can and are sometimes made considerably deeper relative to
20 the outer substrate surface as compared to the oxidation depth of
21 LOCOS. Accordingly, the etching typically produces elongated, deeper
22 and straighter sidewalls than LOCOS. When utilized in a FLASH
23 memory fabrication process, such as described above, the result will be
24 fabrication of discrete and disjointed source regions below the base of

FD6040" 82889250

1 the trenches and in the plateaus or mesa areas of the active area
2 therebetween. Thus, continuous source lines may not be formed in all
3 instances.

4 The invention was motivated in overcoming this particular problem
5 in FLASH memory cell fabrication associated with shallow trench and
6 refill isolation. The artisan will, however, appreciate applicability of the
7 invention in other areas, with the invention only being limited by the
8 accompanying claims appropriately interpreted in accordance with the
9 Doctrine of Equivalents.

10 11 12 SUMMARY OF INVENTION

13 The invention comprises FLASH memory and methods of forming
14 flash memory. In one implementation, a line of floating gates is
15 formed over a semiconductor substrate. The semiconductor substrate is
16 etched to form a series of spaced trenches therein in a line adjacent
17 and along at least a portion of the line of floating gates. At least one
18 conductivity enhancing impurity implant is conducted into the
19 semiconductor substrate at an angle away from normal to a general
20 orientation of the semiconductor substrate to implant at least along
21 sidewalls of the trenches and between the trenches, and a continuous
22 line of source active area is formed within the semiconductor substrate
23 along at least a portion of the line of floating gates.
24

09768878-040901

1 In another implementation, a line of floating gates is formed over
2 a semiconductor substrate. An alternating series of trench isolation
3 regions and active area regions are provided in the semiconductor
4 substrate in a line adjacent and along at least a portion of the line of
5 floating gates. The series of active areas define discrete transistor
6 source areas separated by trench isolation regions. A conductive line
7 is formed over the discrete transistor source areas and trench isolation
8 regions separating same adjacent and along at least a portion of the
9 line of floating gates. The conductive line electrically interconnects the
10 discrete transistor source areas. Source forming conductivity enhancing
11 impurity is provided into the discrete transistor source areas.

12 Other implementations are contemplated.

13 14 15 **BRIEF DESCRIPTION OF THE DRAWINGS**

16 Preferred embodiments of the invention are described below with
17 reference to the following accompanying drawings.

18 Fig. 1 is a diagrammatic top plan of a semiconductor wafer
19 fragment in process in accordance with the invention.

20 Fig. 2 is a view of a semiconductor wafer fragment in process as
21 positionally taken through line 2-2 in Fig. 1.

22 Fig. 3 is a view of the Fig. 2 wafer fragment at a processing
23 step subsequent to that shown by Fig. 2.
24

09768878.040901

1 Fig. 4 is a view of the Fig. 2 wafer fragment at a processing
2 step subsequent to that shown by Fig. 3.

3 Fig. 5 is a view of the Fig. 2 wafer fragment at a processing
4 step subsequent to that shown by Fig. 4.

5 Fig. 6 is a view of an alternate embodiment semiconductor wafer
6 fragment as would positionally appear if taken through cut line 2-2 in
7 Fig. 1.

8 Fig. 7 is a view of the Fig. 6 wafer fragment in a cut taken
9 perpendicularly to that cut depicted by Fig. 6, and intermediate two
10 trench isolation regions.

11 Fig. 8 is a view of a wafer fragment positionally corresponding
12 to that of Fig. 7 exemplifying one exemplary fabrication step used in
13 fabricating the wafer fragment of Fig. 7.

14 Fig. 9 is a view of the Fig. 8 wafer fragment at a processing
15 step subsequent to that shown by Fig. 8.

16 17 18 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

19 This disclosure of the invention is submitted in furtherance of the
20 constitutional purposes of the U.S. Patent Laws "to promote the
21 progress of science and useful arts" (Article 1, Section 8).

22 Referring to Fig. 1, a portion of an array 10 of FLASH memory
23 cells in fabrication is illustrated in top plan view. Such comprises a
24 semiconductor substrate having lines of floating gates 12 and 14 formed

thereover. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above. As illustrated, semiconductor substrate 11 is in the form of a monocrystalline silicon substrate, although SOI and other constructions could also be utilized.

Referring to Figs. 1 and 2, a series of spaced trenches 16 are etched into semiconductor substrate substantially perpendicular to floating gate word lines 12 and 14. Trenches 16 are preferably formed to be at least 2000 Angstroms deep, more preferably 3000 to 4000 Angstroms deep, and have sidewalls normal or within 10° of normal to the general substrate orientation. The area 18 between the trenches thereby comprises spaced lines of active area relative to substrate 11 running between spaced trenches 16. The illustrated sectional cut 2-2 in Fig. 1 is taken adjacent and parallel with lines of floating gates 12 and 14, and will constitute source active area for the respective transistors formed along lines of floating gates 12 and 14. Accordingly, Figs. 1 and 2 can also be considered as depicting in a preferred embodiment an alternating series of trenches and active area regions provided in semiconductor substrate 11 in a line (i.e., line 2-2) running adjacent and

09758878.040901
T06040.88960

1 along at least a portion of lines of floating gates 12 and 14. Active
2 area regions 18 along that line, as depicted in Fig. 2, are thereby
3 spaced or separated by trenches 16.

Sub B 17 Fig. 2 illustrates trenches 16 having been filled with an insulating
4 dielectric material 20, such as high density plasma deposited oxide, and
5 subjected to a planarization step to provide a substantially planar outer
6 surface. At this point in the process, such effectively forms an
7 alternating series of trench isolation regions 22 and active area
8 regions 18 in semiconductor substrate 11 running in a line adjacent and
9 along lines of floating gates 12 and 14. The semiconductor wafer is
10 typically and preferably fabricated to a point as would be depicted in
11 Fig. 2, with the lines of floating gates being fabricated thereafter.
12 Lines of floating gates 12 and 14 preferably constitute a gate dielectric
13 layer (not shown), floating gate regions 23 (Fig. 1), an interpoly
14 dielectric layer (not shown), a conductively doped polysilicon/silicide stack
15 (not shown), and an insulative cap (not shown).
16

17 Drain and source implants in FLASH circuitry fabrication are
18 typically separately conducted and optimized. Accordingly in a preferred
19 implementation of this invention, drain implanting is next performed.
20 A photoresist layer is ideally deposited and patterned to mask the
21 floating gate word lines and source areas therebetween, and to leave
22 the drain areas and isolation regions therebetween outwardly exposed.
23 Exemplary drain areas 24 (Fig. 1) are accordingly left outwardly exposed
24 within active area regions 18. One or more suitable implants are then

09753878-040901

1 provided to provide the desired depth and concentration of conductivity
2 enhancing impurity to form the desired transistor drains within active
3 areas 18 at locations 24.

4 The source regions for the respective floating gate transistors are
5 preferably next fabricated. Specifically, a photoresist layer is preferably
6 deposited and masked to cover the drain areas and lines of floating
7 gates, yet leave the desired source regions exposed in lines running
8 parallel and between the lines of floating gates on their source sides.
9 Accordingly in the depicted Fig. 1 portion, the photoresist would be
10 patterned to cover ideally all but the illustrated area comprising both
11 active area and trench isolation regions running in a line between lines
12 of floating gates 12 and 14. Referring to Fig. 3 and with such mask
13 in place, isolation material 20 from Fig. 2 is removed from trenches 16
14 of trench isolation regions 22. Such removal preferably occurs by
15 conventional oxide etching conducted substantially selective to the
16 material of the semiconductor substrate 11, and is shown such that a
17 majority of said insulating material is etched from the trenches, with
18 such majority in the illustrated Fig. 3 embodiment constituting essentially
19 the entirety of the isolation material previously received therewithin.
20 In the depicted preferred embodiment, such removal from the trenches
21 occurs through a mask opening provided immediately adjacent the line
22 of floating gates along a continuous line of source active area being
23 formed along at least a portion of the line of floating gates, with such
24 area in the example comprising a line of source area for both lines of

09768878-040901

1 floating gates 12 and 14. Thus relative to the array, a series of spaced
2 trenches 16 are provided within semiconductor substrate 11 adjacent and
3 along at least a portion of the line of floating gates, in this example
4 between floating gates 12 and 14.

5 Trench isolation material remains in trenches 16 beneath the lines
6 of floating gates and on the drain sides thereof throughout the array.
7 Preferably, trenches 16 are at least 2000 Angstroms deep, and preferably
8 at least 3000 Angstroms deep, with the sidewalls extending along a line
9 from an outer surface of the semiconductor substrate to the floor of
10 the respective trenches, and being straight along a majority of the
11 length of that line. This is understood to be contrary to the prior art
12 LOCOS isolation wherein trenches left after etching of LOCOS field
13 oxide along the source areas leaves trenches less than 2000 Angstroms
14 deep and with largely curved sidewalls. In accordance with one aspect
15 of the invention, suitable conductivity enhancing impurity is implanted
16 into the semiconductor substrate to beneath the trenches, along sidewalls
17 of the trenches, and between the trenches, and forming therefrom a
18 continuous line of source active area within the semiconductor substrate
19 along at least a portion of the line of floating gates. Several
20 implementations are considered in accordance with the invention and as
21 may be impacted by trench depth and shape, or other processing
22 concerns.

23 Consider for example Fig. 4. In accordance with one
24 implementation, at least one conductivity enhancing impurity implant is

1 conducted into semiconductor substrate 11 at an angle away from
2 normal (arrows 32) to a general orientation (i.e., along line 33) of the
3 semiconductor substrate. Such is depicted by arrows 28 which are
4 illustrated as being other than perpendicular to a general orientation of
5 the substrate such as depicted by the generally planar outer surface of
6 the substrate of Fig. 2. In one implementation, such will implant at
7 least along sidewalls of trenches 16 and between the trenches in active
8 areas 18. If the implant angle is suitably close to normal, and
9 depending upon the aspect ratio of trenches 16, such may result in a
10 continuous line 30 of implanted source active area within semiconductor
11 substrate 11 along and between lines of floating gates 12 and 14. In
12 some instances, the trenches may be effectively deep to preclude
13 forming a continuous implant region at bases of the trenches from a
14 desired angled implant. Accordingly in such and other instances, an
15 implementation of the invention further comprises conducting at least
16 one conductivity enhancing impurity implant into the semiconductor
17 substrate at an angle normal to the general orientation of the
18 semiconductor substrate. Such is depicted by arrows 32 in Fig. 4.
19 Accordingly, multiple implants of the same or different impurities can
20 be conducted relative to the same or different angles in accordance with
21 the invention.

22 Another preferred embodiment incorporating implementations of the
23 invention is described with reference to Fig. 5. Like numerals from the
24 first-described embodiment have been utilized where applicable, with

09758878-040901

1 differences being indicated by the suffix "a" or with different numerals.
2 Here, spaced trenches 16a are fabricated to comprise sidewall 17 having
3 portions thereof angled at least 15° from a direction 32 normal to a
4 general orientation of semiconductor substrate 11. More preferably,
5 sidewall portions are angled at greater than 15° from normal, such as
6 at least 20° from normal, at least 30° from normal, and at least 40°
7 from normal. Such angling of sidewalls of etched trenches may enable
8 one or more desired source-forming implants to be conducted only at
9 an angle normal (along line 32) to the general orientation of the
10 semiconductor substrate. Alternately and more preferred however, ion
11 implanting with respect to the embodiment of Fig. 5 includes multiple
12 implants conducted both normal and at an angle away from normal in
13 the circuitry fabrication to form a continuously running source line 30a.
14 Such is believed to produce a more homogenous implant along the
15 length of continuous source line being formed. Example implantings
16 include both phosphorus at a dose from 1 - 3 E15 ions/cm², energy at
17 30 - 70 keV, and arsenic at a dose from 0.5 - 3 E14 ions/cm², energy
18 at 20 - 60 keV. An insulative spacer layer in either of the
19 above-described embodiments would thereafter be deposited to produce
20 insulating spacers (not shown) about the drain and source sides of the
21 lines of floating gates.

22 Another implementation is described with reference to Figs. 6-7.
23 Like numerals from the first-described embodiment are utilized where
24 appropriate, with differences being indicated with the suffix "b" or with

1 The Figs. 6 and 7 construction could be fabricated in any of a
2 number of manners. Further, alternate embodiments to that depicted
3 in Figs. 6 and 7 are of course contemplated, with the invention only
4 being limited by the accompanying claims appropriately interpreted in
5 accordance with the Doctrine of Equivalents. In one implementation,
6 processing can occur as described in the first-described embodiment to
7 the point of forming a source line mask opening in a layer of
8 photoresist along and between lines of floating gates 12 and 14.
9 Further, the patterning of the lines of floating gates is preferably such
10 that the illustrated bottom gate dielectric layer 43 is not etched in
11 initially forming the lines. Desired ion implanting of a source forming
12 impurity is conducted through the source line mask openings.
13 Implanting occurring within regions 20 is of no consequence. Further,
14 gate dielectric material overlying the source areas is etched away
15 through the source line mask openings.

16 The photoresist is subsequently stripped, and an electrically
17 insulative spacer forming layer is deposited over the entirety of the
18 wafer. Such is ideally comprised of a different material than gate
19 dielectric layer 43 of lines 12 and 14. Circuitry peripheral to the array
20 is then preferably masked such that the entirety of the array remains
21 open. Spacers for the lines of floating gates within the array, such as
22 the depicted spacers 42 in Fig. 7, are then formed by anisotropic
23 etching to electrically isolate the sides of the lines of floating gates.
24 Such preferably does not occur yet in the periphery which is why it is

09768878-040901

1 masked, as the preferred subsequently deposited polysilicon would
2 otherwise result in polysilicon on monocrystalline silicon in the preferred
3 embodiment over the peripheral transistor and other circuitry active
4 areas. Unetched material 43 over drain locations 24 will separate
5 monocrystalline silicon from polysilicon in this example embodiment.
6 Alternately, if the peripheral gates are also initially formed such that
7 the bottom gate dielectric layer is not etched and comprises a material
8 different from the spacer layer, this material will separate polysilicon
9 from monocrystalline silicon such that masking of the spacer forming
10 layer in the periphery is immaterial.

11 The photoresist would then be stripped, and conductively doped
12 polysilicon and silicide or refractive metal thereafter globally deposited
13 over the substrate. Such would subsequently be patterned to produce
14 the exemplary illustrated line 40 of Fig. 7. Such patterning and etch
15 with leaving the spacer layer unetched in the periphery circuitry provides
16 a convenient etch stop to remove the source strapping polysilicon/silicide
17 layer outwardly of the array. Such processing as compared to the
18 first-described embodiment does, however, require at least two additional
19 masks in a first mask for the periphery during the spacer etch and in
20 a second subsequent mask in formation of source strapping lines 40.
21 Further, in this and the subsequent described embodiment, conductivity
22 enhancing impurity provided within semiconductive material layer 38 can
23 out diffuse into the discrete transistor source areas, thereby facilitating
24 formation of source regions 30b within the active areas.

09768878-040901

1 Consider now yet another exemplary implementation 10c for
2 fabrication of the Fig. 7 and other embodiments as described with
3 reference to Figs. 8 and 9. Like numerals from the third-described
4 embodiment are utilized where appropriate, with differences being
5 indicated with the suffix "c" or with different numerals. In this
6 embodiment, fabrication occurs to a point of word line formation and
7 drain implant as in the immediately above described embodiment. Yet
8 in this one example, the gate dielectric layer is patterned with the
9 initial patterning of lines 12 and 14. Then, an insulative sidewall
10 forming layer 46 is deposited over the wafer and lines of floating gates.
11 A layer of photoresist 48 is then deposited and patterned to only
12 expose the source sides of the lines of floating gates, as shown.

13 Referring to Fig. 9, insulative sidewall spacers 42 are formed on
14 the source sides of lines of floating gates 12 and 14 by anisotropically
15 etching insulative sidewall forming layer 46. More broadly considered,
16 an insulative sidewall spacer is formed on one of the source side or
17 the drain side of the line of floating gates before the other sidewall
18 spacer on the opposing side is formed. In this particular embodiment,
19 the source side insulative spacer is shown being formed before the drain
20 side (not shown in Fig. 9), although the reverse could also occur. In
21 another considered aspect of the invention, in one anisotropic etching
22 step of the insulating sidewall forming layer, an insulative sidewall
23 spacer is formed on only one of the source side and the drain side,
24 and not the other, as depicted by example in Fig. 9. In another

09768878-040901

1 anisotropic etching step, an insulative sidewall spacer can be formed on
2 the opposing drain side. Alternately, no insulative sidewall spacer is
3 ever formed on the opposing drain side.

4 In accordance with the preferred aspect of the Fig. 9 depicted
5 embodiment, ion implanting is conducted before removing photoresist
6 layer 48 to provide conductivity enhancing impurity implant 30c into the
7 respective active area source regions. Subsequently, the photoresist is
8 stripped and the conductive line forming material, preferably conductively
9 doped semiconductive material, is deposited and patterned to form
10 lines 40 (Fig. 7). Alternately but less preferred, the source implanting
11 with respect to the construction of Fig. 9 can be eliminated, with
12 source forming implant being totally relied upon by out-diffusion of
13 conductivity enhancing impurity from the deposited doped semiconductive
14 material of the line forming layer. As alluded to above, subsequent
15 processing may or may not form spacers on the drain side of the
16 floating gates, for example commensurate with or separately from
17 forming spacers in connection with the peripheral circuitry.

18 In compliance with the statute, the invention has been described
19 in language more or less specific as to structural and methodical
20 features. It is to be understood, however, that the invention is not
21 limited to the specific features shown and described, since the means
22 herein disclosed comprise preferred forms of putting the invention into
23 effect. The invention is, therefore, claimed in any of its forms or
24

19

09768878-040901

1 modifications within the proper scope of the appended claims
2 appropriately interpreted in accordance with the doctrine of equivalents.
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

20